IN THE CLAIMS:

Please amend the claims as follows:

1. (Original) A CPU contained LSI comprising:

a contained CPU;

a first bus connected to the contained CPU;

a second bus connected to an external CPU; and

a bus adjusting circuit disposed between the first bus and the second bus to exclusively control accesses of the external CPU and the contained CPU to a device connected to the first bus and connect the second bus to the first bus only when the external CPU is permitted to access the device connected to the first bus.

2. (Original) A CPU contained LSI according to claim 1, wherein, when an access request to the device connected to the first bus from the external CPU is generated during an access to the device connected to the first bus by the contained CPU, the bus adjusting circuit transmits a bus release request signal to the contained CPU and transmits a wait signal to the external CPU, and when the bus adjusting circuit receives a bus release completion signal from the contained CPU, the bus adjusting circuit releases the wait signal to permit the external CPU to access the device connected to the first bus.

3. (Currently amended) A CPU contained LSI according to claim 2, wherein when a ~~the~~ stop of the operation of the contained CPU is set, the bus adjusting circuit permits the external CPU to access the device connected to the first bus without transmitting the bus release request signal to the contained CPU.

4. (Original) A CPU contained LSI according to any one of claims 1 to 3, wherein a common memory connected to the first bus is provided.

5. (Currently amended) A CPU contained LSI according to any one of claims 1 to 4, wherein a memory device connected to the first ~~device~~ bus is provided for storing a program for operating the CPU contained LSI.

6. (Original) A CPU contained LSI according to any one of claims 1 to 5, wherein the bus adjusting circuit is provided with an interrupt control circuit for informing of an interruption between the contained CPU and the external CPU.

7. (Currently amended) A CPU contained LSI according to claim 6, wherein the interrupt control circuit includes an interrupt factor register having a plurality of bits in which the allocation and setting of bits of an interrupt factor are programmable and a circuit for outputting ~~the bit or of the interrupt factor register as~~ an interrupt signal.

8. (Original) A CPU contained LSI according to claim 5, wherein the memory device connected to the first bus is a RAM and when the CPU contained LSI is started, the external CPU loads the RAM with a program for operating the contained CPU from an external memory connected to the second bus.

9. (Original) A CPU contained LSI according to claim 8, wherein the bus adjusting circuit includes a writing address register and a writing data register, and when the external CPU loads the RAM with the program for operating the contained CPU, the external CPU sets the

address of the RAM to the writing address register and writes data to be written in the RAM in the writing data register.

10. (Original) A CPU contained LSI according to claim 9, wherein the writing address register is incremented every time data is written in the writing data register.

11. (Currently amended) A CPU contained LSI comprising:

a first contained CPU;

a second ~~contained~~ CPU;

a first bus connected to the first contained CPU;

a second bus connected to the second ~~contained~~ CPU ; and

a bus adjusting circuit disposed between the first bus and the second bus to exclusively control accesses of the second ~~contained~~ CPU and the first contained CPU to a device connected to the first bus and connect the second bus to the first bus only when the second ~~contained~~ CPU is permitted to access the device connected to the first bus.

12. (New) A CPU contained LSI according to claim 1, wherein the external CPU has priority over the contained CPU for accessing the device connected to the first bus.

13. (New) A CPU contained LSI according to claim 11, wherein the second CPU has priority over the first contained CPU for accessing the device connected to the first bus.